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Abstract

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OF THE SERIES RESONANT CONVERTER
OPERATING ABOVE RESONANCE

by Francis Aloysius Fahy
Capt, USAF

A thesis submitted in partial fulfillment
of the requirements for the degree of

Master of Science

University of Washington

1988

Chairperson of the Supervisory Committee:
Professor Thomas H. Sloane
Department of Electrical Engineering

Design methods for optimizing efficency of the series resonant converter (SRC) operating above resonance are presented. Included in the power loss analysis is the development of expressions for individual component power losses as a function of the transformer turn ratio n, the circuit characteristic impedance R_o, and other design variables. Results of the operating efficiency are graphically represented as a function of n and R_o for a hypothetical SRC circuit with 100W output power and 50KHz switching frequency with discussion of results following.

(52 pages)

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in

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Approved by Thomas Lawrence
(Chairperson of Supervisory Committee)

Program Authorized
to Offer Degree Electrical Engineering

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CHAPTER 1

INTRODUCTION

In the past several years, there have been a number of technical papers written to aide the design of the series resonant converter (SRC). Francis C. Schwarz introduced the SRC as a converter with a high power/weight ratio and efficient semiconductor switching characteristics [1]. The typically high operating efficiency of the SRC results from the reduction of switching losses. The reduction of switching losses allows very high frequency operation which provides the advantage of size reduction of the components. The reduction in component sizing ultimately reduces the weight of the converter. These advantages of the SRC have been utilized in aerospace power supply system applications.

After Schwarz presented the improved SRC, other research followed with the purpose of obtaining a more complete analysis of the SRC [2]. Stuart and King modified the analysis of Schwarz and derived closed-form steady-state equations for the SRC [3]. Results of their research includes expressions for normalized currents and voltages as a function of the 'retard angle', often called the diode conduction angle. Vorperian and Cuk followed with a rigorous dc analysis of the SRC which expressed the gain or

dc-to-dc conversion ratio as a function of the switching frequency, resonant frequency, inductance, and load resistance [4]. Most recently, Witulski and Erickson have considered steady-state SRC operation with the intent to minimize component stress [5]. Their analysis of converter operation and component stress is based on a normalized output-plane model. With the same motivation as the aforementioned authors, to aid the design of the SRC, this thesis seeks to develop design methodologies for maximizing steady-state operating efficiency of the SRC above resonance.

The primary task of this thesis is to develop an analytical expression for the efficiency of the SRC as a function of the transformer turn ratio n and the characteristic impedance R_o of the series L-C resonant circuit. To determine this efficiency, a systematic analysis of the power losses for the individual components is required. Due to the series configuration of the SRC, the same current flows through all components. Determination of component losses as a function of n and R_o can be simplified if the series current can be expressed as a function of n and R_o. Analytic models must be utilized to develop expressions for the power losses in the individual components.

Before developing these expressions relating losses of each component to the design parameters n and R_o, the basic operation of the SRC must be understood. In Chapter 2 a general discussion of converter waveforms and operation above resonance is presented. Chapter 3 introduces and defines the design parameters the normalized output-plane analytical model. Chapters 4 contains development of loss expressions for each of the components of the SRC. In Chapter 5, total power losses are computed for a specific converter configuration. The efficiency of this particular converter is graphically represented as a function of the transformer turn ratio n, and tank characteristic impedance R_o. Also included in Chapter 5 is detailed explanation of the analytical results and suggestions for design strategies which produce SRC's which operate with maximum efficiency.

CHAPTER 2

ABOVE-RESONANCE CONVERTER OPERATION

The topology of the series resonant converter (SRC) considered here is shown in Figure 2.1(a). The SRC, a type of dc-to-dc converter, produces a dc output voltage V_O across the load resistance R_L. Input power is provided by the two equal-valued input voltage sources V_{G1} and V_{G2}. The converter is composed of two switching transistors Q_1 and Q_2 with corresponding anti-parallel diodes D_1 and D_2, a series inductance L and capacitance C that compose the L-C resonant tank circuit, an ideal two-winding transformer, a rectifying diode bridge DB_1-DB_4, an output filter capacitor C_O, and a load resistance R_L. In fabricating the SRC, the two separate voltage sources V_{G1} and V_{G2} are derived from a single voltage source V_{IN} by using a pair of capacitors C_{IN} as a voltage divider as seen in Figure 2.1(b). Square-wave voltage excitation of the L-C tank circuit is created by switching transistors Q_1 and Q_2 with a 50% duty cycle to produce ac currents in the L-C resonant tank circuit. The L-C tank current i_x is transformed and rectified to create the desired dc output current I_O. The output filter capacitor C_O provides the filtering necessary to provide an output voltage which is essentially purely dc.

Assuming the SRC components to be ideal or lossless,

the values of the dc output voltage V_o and the output current I_o are dependent on the input voltage V_s, where

$$V_s = V_{s1} = V_{s2} \qquad (2.1),$$

the natural resonant frequency fo of the L-C tank circuit, where

$$f_o = 1/[2\pi(LC)^{1/2}] \qquad (2.2),$$

the switching frequency f_s of the transistors, the characteristic impedance R_o of the tank circuit, where

$$R_o = (L/C)^{1/2} \qquad (2.3),$$

the transformer turn ratio n defined by the number of primary turns N_p and the number of secondary turns N_s as

$$n = N_s/N_p \qquad (2.4),$$

and the load resistance R_L.

By defining the normalized voltage conversion ratio M and the normalized output current J as,

$$M = V_o/nV_s \qquad (2.5)[5],$$

where M < 1, and

$$J = nR_o I_o / V_s \qquad (2.6)[5],$$

many expressions describing SRC operation can be generalized.

When the L-C tank circuit is excited by a square-wave voltage with a switching frequency f_s which is higher than the natural resonant frequency fo of the L-C tank, the sequence of events for steady-state operation is:

(a) Initially, the tank current i_x is negative. Transistor Q_1 is ON and Q_2 is off. Because i_x is negative, diode D_1 is ON and V_{s1} is connected through diode D_1 to the series L-C circuit producing the circuit topology shown in Figure 2.2(a). The voltage across the series L-C circuit V_T is

$$V_T = V_s + V_o/n \qquad (2.7),$$

During this period, the tank current i_x is flowing from the series L-C circuit back into the voltage source V_{s1}. At a time defined as T_A, the sinusoidal current in the series L-C circuit reaches an instantaneous value of zero.

(b) Between time T_a and $T_s/2$, the tank current is positive and transistor Q_1 is ON. Thus, V_{s1} is connected to the series L-C circuit, the circuit configuration is shown in Figure 2.2(b). The positive tank current i_x conducts through the switching transistor Q_1 and rectifying diode bridge diodes DB_1 and DB_3. The voltage across the the L-C tank V_T is,

$$V_T = V_s - V_o/n \qquad (2.8).$$

Current is flowing from the voltage source V_{s1} over this interval.

(c) To begin the second half of the switching period, transistor Q_1 is turned OFF forcing the continuous tank current, which is positive, to commutate diode D_1 ON. The voltage source V_{s2} is connected to the tank circuit through D_1. The circuit topology during this interval is shown in Figure 2.2(c). The voltage across the L-C tank V_T is,

$$V_T = -V_s - V_o/n \qquad (2.9).$$

In this interval, the tank current i_x flows through anti-parallel diode D_2 and bridge diodes DB_1 and DB_3 and is half-wave symmetrical to the current previously conducted

in diode D_1. Current is being supplied to V_{dc}. Eventually, as in the case of current conduction in diode D_1 during the preceding half cycle, i_x reaches an instantaneous value of zero.

(d) In the final interval of the switching cycle, i_x is negative while Q_1 is ON. The equivalent circuit during this interval is seen in Figure 2.2(d). Current is flowing through Q_2 and DB_2 and DB_4. The current supplied by V_{dc} to the series L-C circuit and is half-wave symmetrical to the current conducted in Q_1 in the previous half cycle. The voltage V_T is,

$$V_T = -V_o + V_o/n \qquad (2.10).$$

This interval ends when Q_2 is turned OFF. When Q_2 is turned OFF, the current in the resonant tank is negative and is equal to the value used in the beginning of the analysis (i.e. (a)).

The switching sequence briefly presented above results in two possible waveforms for the L-C tank current i_x depending on circuit parameters. The two possibilities are shown in Figure 2.3. In either case, the anti-parallel diode always conducts current before its respective switching transistor [4]. Thus, the conduction sequence

for above resonance excitation over half a switching period is D_1, Q_1, or D_2, Q_2. By sectionalizing the waveform according to the conducting switching device for the corresponding segment (i.e., Q_1, Q_2, D_1, or D_2), the current waveform can be described as piecewise sinusoidal.

For a given output voltage V_O, the expression for the L-C tank current i_x waveform is a function of V_S, M, J, R_O, f_O, and f_S. In preparation for expressing the tank current i_x as a function of these arguments, they are now defined. The angular resonant frequency w_O is defined as

$$w_O = 2\pi f_O = (LC)^{-1/2} \qquad (2.11),$$

and the ON-time of the anti-parallel diode T_A is defined as

$$T_A = (1/w_O)\ \arccos[(1 - M^2 - KM^2)/(MK + M + 1)] \qquad (2.12)[6].$$

Also requiring definition are the switching period T_S defined as,

$$T_S = 1/f_S \qquad (2.13),$$

and circuit parameter K, which is

$$K = (Jf_o\pi)/(2f_sM) \qquad (2.14).$$

Each segment of the current waveform can be expressed as a sinusoidal function with a frequency equal to the angular resonant frequency (w_o) of the L-C tank circuit over a closed interval.

During the time interval when D_1 or Q_1 conduct current ($0 < t < T_s/2$), the SRC circuit configuration is shown in Figure 2.2(a) and (b). The expression for the segment of the current waveform characterized by current conduction in the anti-parallel diode D_1 is

$$i_x(t) = (V_s/R_o)[1 + M(K + 1)] \sin[w_o(t - T_A)]$$
$$0 < t < T_A \qquad (2.15)[6],$$

The expression for the segment of the current waveform characterized by current conduction in the switching transistor Q1 is

$$i_x(t) = (V_s/R_o)[1 + M(K - 1)] \sin[w_o(t - T_A)]$$
$$T_A < t < T_s/2 \quad (2.16)[6].$$

During the second half of the switching period characterized by current conduction in D_2 and Q_2, the SRC

circuit configuration is shown in Figure 2.2(c) and (d). The half-wave symmetry of i_x permits utilization of equations (2.15) and (2.16) for the current conduction in D_e and Q_e respectively by changing the sign of the equations.

As stated earlier, the waveform for the L-C tank current i_x has two possible shapes depending on the circuit parameters M and K [6]. The difference between the current waveforms shown in Figure 2.3, is that the peak of the current waveform occurs before the current commutates from the switching transistor to the opposing anti-parallel diode in Figure 2.3(a) or at the instant of commutation as in Figure 2.3(b). The expression determining the value of the peak L-C tank current I_{xp} developed by Vorperian and Cuk states the following conditions, if

$$1 - M - KM^2 < 0 \qquad (2.17),$$

then

$$I_{xp} = (V_g/R_o)(1 - M + MK) \qquad (2.18)[6],$$

which corresponds to I_{xp} occurring before current commutation as in Figure 2.3(a).

If however

$$1 - M - KM^2 > 0 \qquad (2.19),$$

then

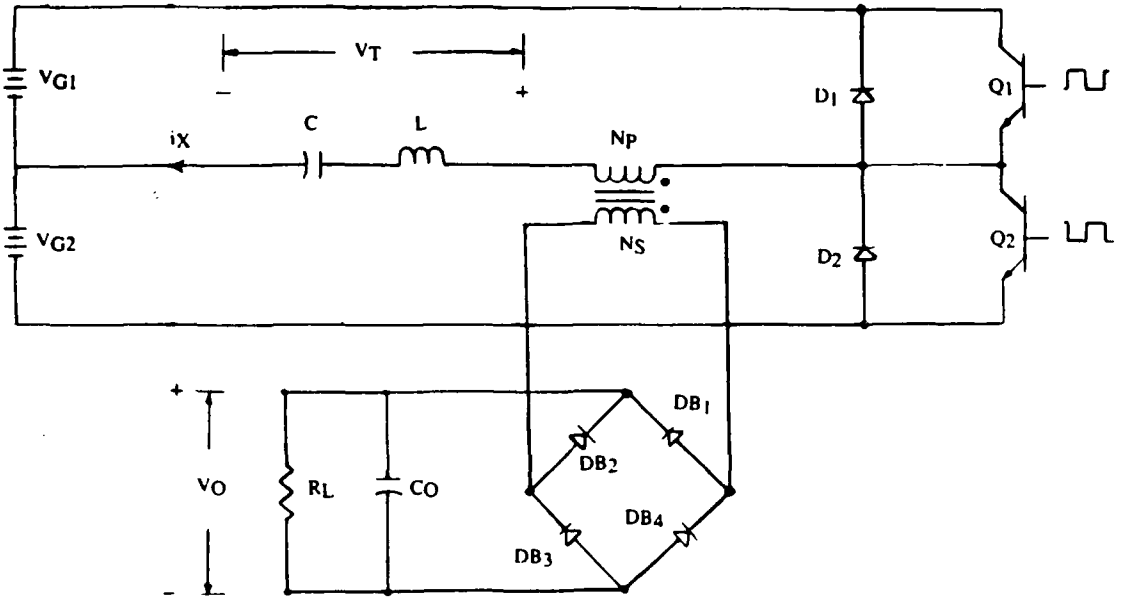
$$I_{xp} = (V_o/R_o)[(1 - M^2)MK(MK + 2)]^{1/2} \qquad (2.20)[6],$$

which corresponds to I_{xp} occurring at the instant of commutation as in Figure 2.3(b). Determination of the peak tank current is important for the evaluation of component stress as well as peak flux in the resonant inductor L.

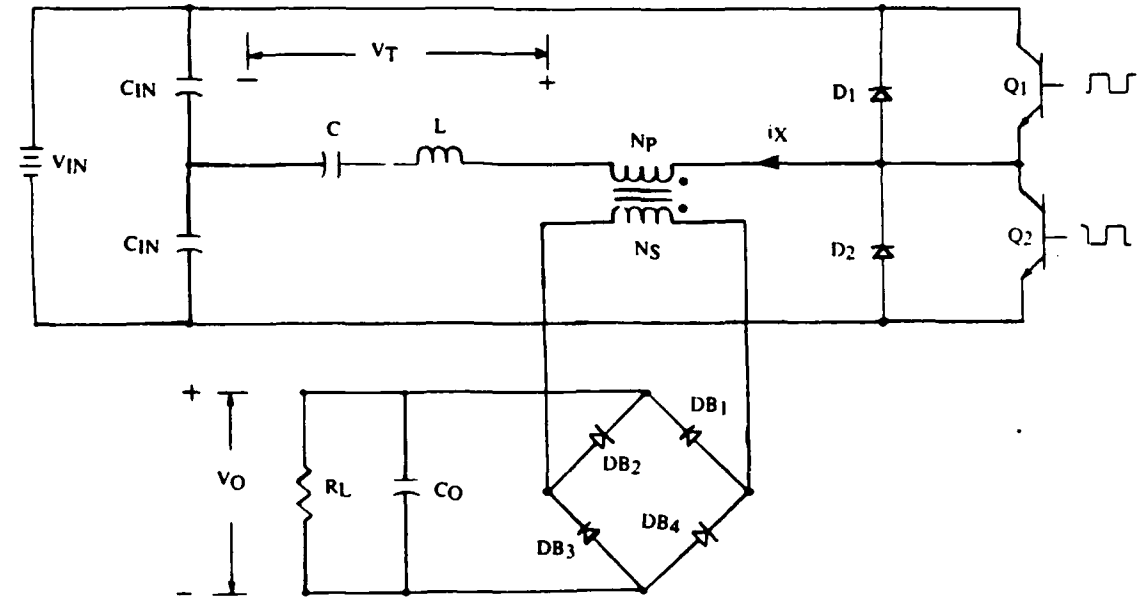
The output voltage V_o of the SRC is dependent on the waveform of i_x, the load resistance R_L and the transformer turn ratio n. The value of the average output current I_o is the average of the reflected and full-wave rectified L-C tank current. In steady-state operation, there can be no average current in the output filter capacitor C_o, thus the average dc output voltage V_o is the product of the average output current I_o and the load resistance R_L.

In recent technical papers, the normalized voltage conversion ratio M, has been used to describe the SRC operation. Analytical models and transcendental equations used to solve for M have been developed by Vorperian and

Cuk[4], and Witulski and Erickson[5]. Graphic representation of the normalized voltage conversion ratio for operation above resonance as a function of the normalized frequency and normalized load resistance R is shown in Figure 2.4 [6].



(a)



(b)

Figure 2.1 Topologies of Series Resonant Converter

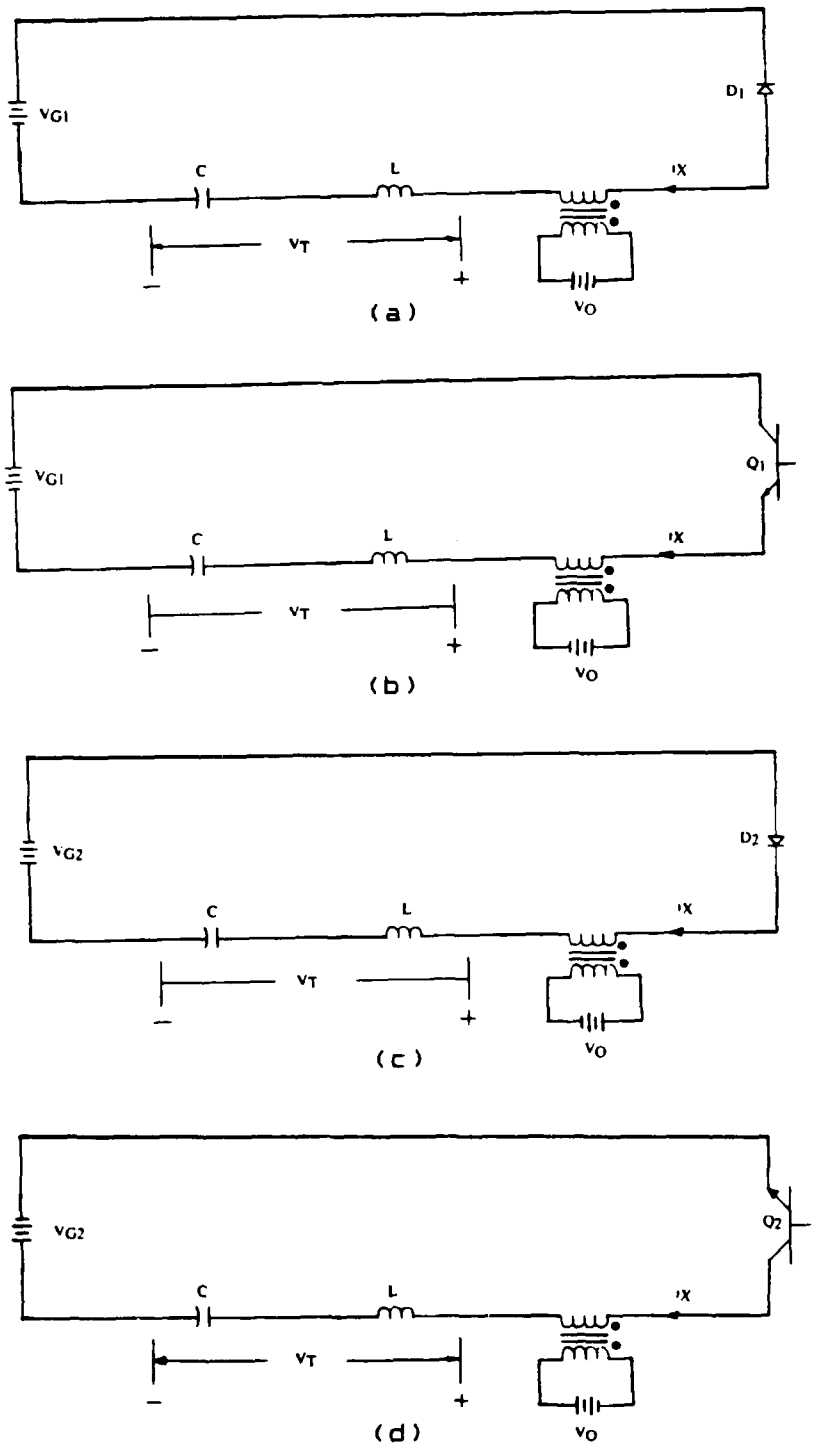


Figure 2.2 Circuit Switching Configurations

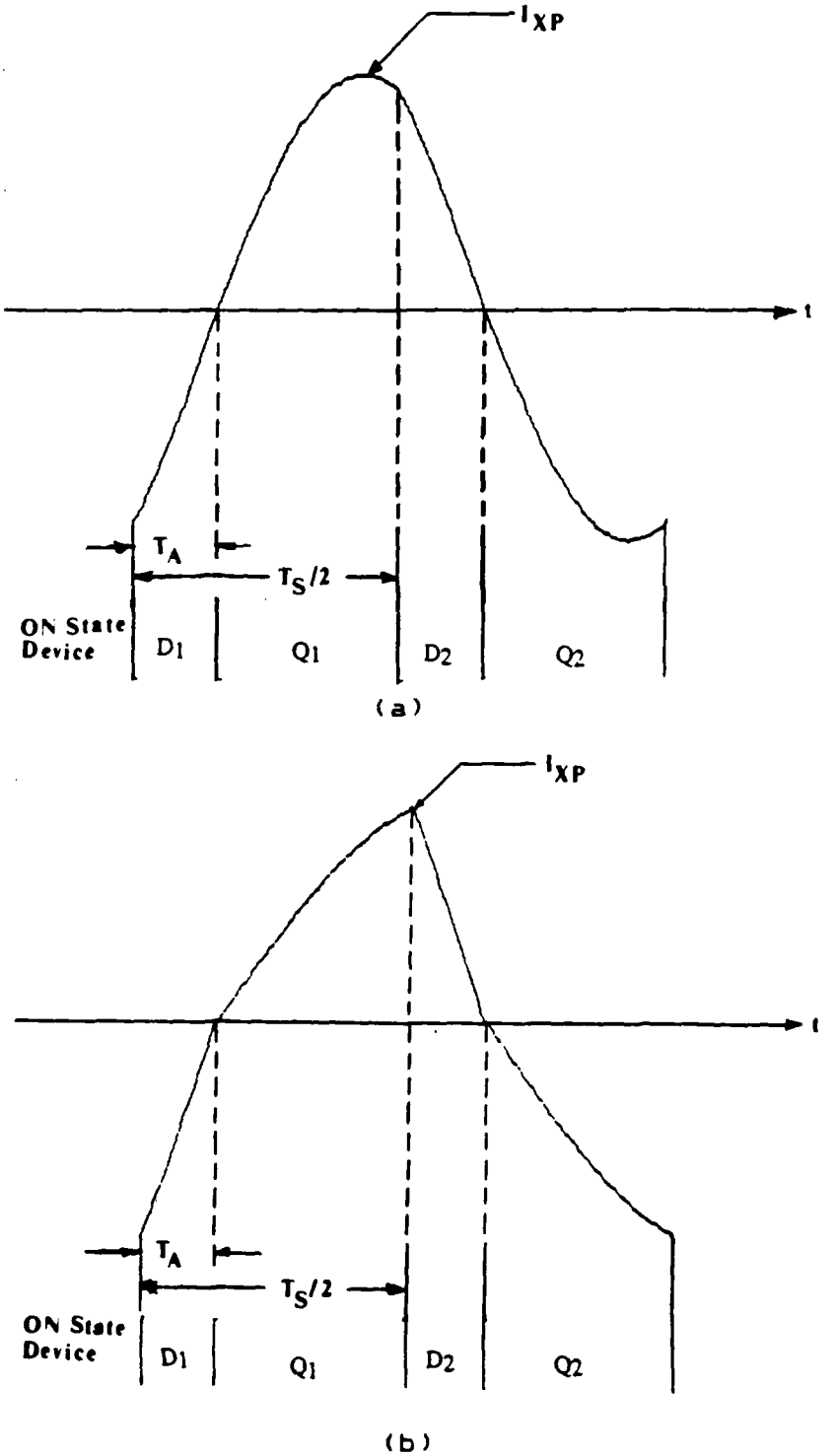


Figure 2.3 Series L-C Circuit Current Waveforms

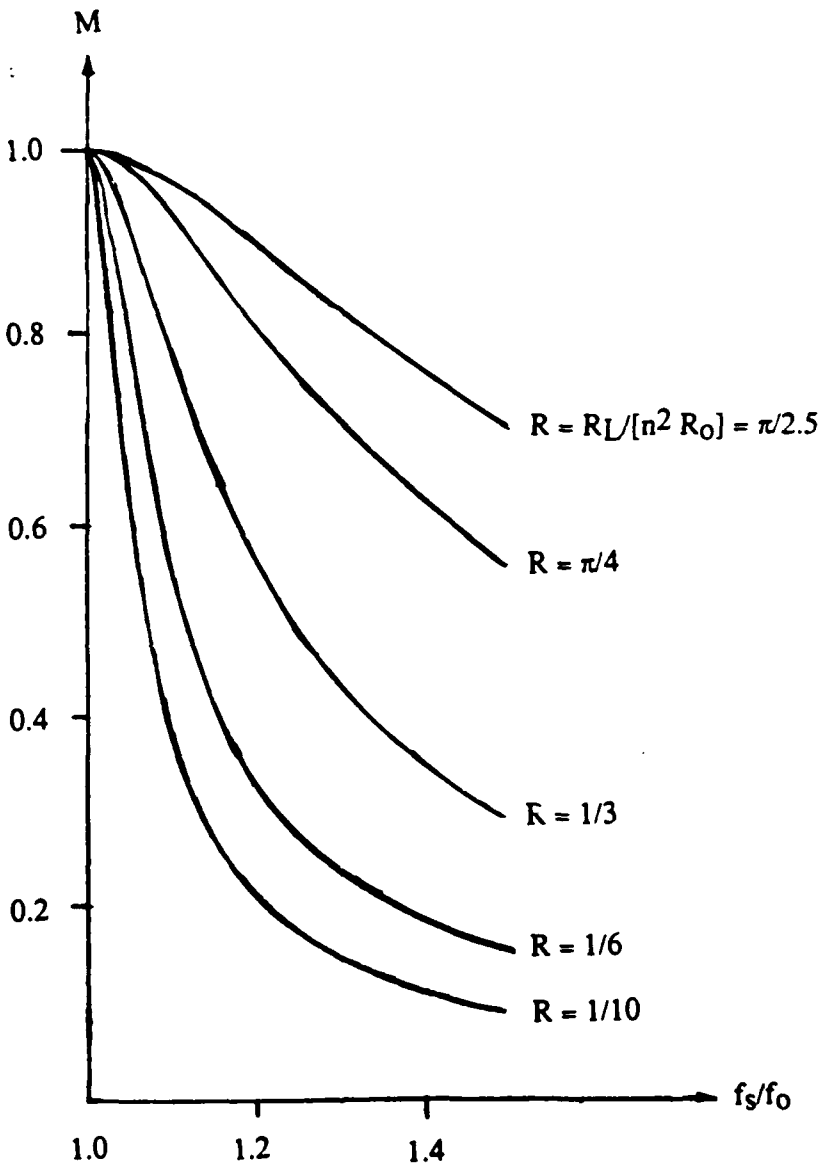


Figure 2.4 Normalized Voltage Conversion Ratio

CHAPTER 3

DESIGN VARIABLES AND ANALYSIS METHOD

The purpose of this research is to analyze the efficiency of the series resonant converter (SRC) operating above resonance by determining the power losses for each of the circuit components. Losses to be computed include conduction and switching losses of semiconductor devices, losses in the series resonant or tank capacitor C, and the core and winding losses of the series resonant or tank inductor L. Expressions for component losses are developed as functions of the transformer turn ratio n, the characteristic impedance R_o.

For the analysis of operating efficient of the SRC, the user-specified dependent variables are defined to be the input voltage V_s, output voltage V_o, and output current I_o. Independent design variables are the characteristic impedance R_o of tank circuit, switching frequency f_s, and transformer turn ratio n. Aside from operating efficiency which evaluated here, other important design criteria include energy storage in the inductor L and capacitor C and component stress.

Final analysis of converter efficiency requires development of expressions as functions of the independent

design variables for the peak inductor current, rms tank current, instantaneous tank current, and average current through switching transistors and anti-parallel diodes. The most suitable method for examining the domain of the independent variables is the the normalized output-plane model developed by Witulski and Erickson [5]. The normalized output-plane model defines an operating point of the converter to be on the M-versus-J plane. The the M axis represents the normalized voltage conversion ratio which has been defined in (2.5). The Y axis of this plane represents values of the normalized output current J previously defined in (2.6). The normalized output-plane model provides uncomplicated solutions for values of inductance L and capacitance C, component stress, peak currents, and resonant frequency. These values are all necessary for evaluation of component losses.

Mapping operating points on the M-versus-J plane from the design variables n and R_o is quite simple. Conversion of the ordered pair of n and R_o for a particular V_s, V_o, and I_o provides unique paired values of M and J by using equations (2.5) and (2.6).

The normalized frequency is computed from an iterative solution of the transcendental equation (3.1) for a particular operating point on the M-versus-J output-

plane.

$$J = (2/\gamma)(1 + [1 + (1 - M^2) \times \tan^2(\gamma/2)]^{1/2}) \quad (3.1)[5].$$

This normalized switching frequency is related to the switching frequency by

$$\gamma = \pi f_o / f_s \quad (3.2).$$

For a particular switching frequency f_s, the values of f_o, L, and C, can be calculated as

$$f_o = f_s \gamma / \pi \quad (3.3),$$

$$L = R_o / (2\pi f_o) \quad (3.4),$$

and

$$C = 1/(2\pi f_o R_o) \quad (3.5).$$

These values are necessary for the evaluation of operating efficiency and the fabrication of an actual SRC because certain expressions concerning component loss cannot be stated solely as functions of R_o and n.

Once design variables are known, calculation of

component and total power losses for the resonant circuit operating under these particular parameters is possible. These losses are developed in Chapter 4 which follows.

CHAPTER 4

COMPONENT LOSS EXPRESSIONS

To simplify the analysis and development of expressions for the individual component losses, it is assumed that the circuit waveforms are not significantly affected by component and circuit parasitics. As shown in Chapter 2, the waveforms of the SRC operated above resonance exhibit half-wave symmetry. Based on this symmetry, component power loss can be calculated over either half the switching period.

4.1 SWITCHING TRANSISTOR LOSSES

In the analysis of power losses for switching transistors Q_1 and Q_2 of Figure 2.1, two types of losses are considered. The first type is conduction loss occurring during the ON time of the transistor. The second type of loss considered is transistor switching losses which occur during the transistor's transition between the ON and OFF states. Losses associated with the turning ON of the transistor during the transition between the OFF and ON states are assumed negligible. Justification of this assumption is based on the waveform of i_x. Review of Figure 2.3 shows the natural commutation of the tank current i_x from the anti-parallel diode to its

corresponding switching transistor. In this commutation, the diode is turning OFF at zero current and the transistor is turning ON with no collector current.

Due to the half-wave symmetry of i_x, the collector current i_C waveform in each switching transistors is identical. The expression for the conduction loss of both transistors $P_{Q,ON}$, is the integral of the product of the transistor collector-emitter voltage $v_{CE}(t)$ and the instantaneous current through each transistor $i_x(t)$ over the entire ON time t_{ON} multiplied by twice the reciprocal of the switching period. The expression for $P_{Q,ON}$ is

$$P_{Q,ON} = (2/T_S)\int^{t_{ON}} v_{CE}(t)\, i_x(t)\, dt \qquad (4.1).$$

Reviewing SRC operation in Chapter 2, the limits of equation (2.16) show that each of the switching transistors are in the ON state for only a portion of the switching period. Assuming $v_{CE}(t)$ is time independent when the transistor is ON, the collector-emitter saturation voltage V_{CESAT} replaces $v_{CE}(t)$ in (4.1). By substituting Vcesat for $v_{CE}(t)$ in equation (4.1), the new expression for $P_{Q,ON}$ is

$$P_{Q,ON} = (2/T_S)\, V_{CESAT} \int_{T_A}^{T_S/2} i_x(t)\, dt \qquad (4.2).$$

It is possible to compute $P_{Q,ON}$ by integrating (4.2). Since collector current exists only during the ON time, this integration is equivalent to calculating the average switching transistor current I_Q, where

$$I_Q = (2/T_S)\int_{T_A}^{T_S/2} i_x(t)dt \qquad (4.3).$$

However, given an operating point on the M-versus-J plane and switching period, a less cumbersome calculation is given.

Adapting the work of Vorperian and Cuk for above resonant excitation [4], the normalized voltage conversion ratio M can be expressed a function of the average switching transistor current I_Q and the average anti-parallel diode current I_D, such that

$$M = (I_Q - I_D)/(I_Q + I_D) \qquad (4.4),$$

where I_Q is previously defined in equation (4.3), and

$$I_D = (2/T_S)\int_{0}^{T_A} i_x(t)dt \qquad (4.5).$$

By adding the integer one to both sides of (4.4), the results are

$$M + 1 = (2I_a)/(I_a + I_b) \qquad (4.6).$$

Equating the sum of the I_a and I_b to be the average output current I_o multiplied by the transformer turn ratio n such that

$$I_a + I_b = nI_o \qquad (4.7),$$

and substituting (4.7) into (4.6), results in a new expression for the average switching transistor current,

$$I_a = nI_o(M + 1)/2 \qquad (4.8).$$

Substituting the expression for M given in (2.5) into (4.8) provides an expression for I_a as a function of the circuit parameters n, I_o, V_a, and V_o, where

$$I_a = (V_o/V_a + n)I_o/2 \qquad (4.9).$$

Since n, I_o, V_a, and V_o are user-defined circuit parameters, the value for I_a has been determined without integrating equation (4.3). Therefore, $P_{a,ON}$ is simply

$$P_{a,ON} = V_{CESAT}I_o(V_o/V_a + n)/2 \qquad (4.10).$$

Calculation of switching losses requires evaluation of

the instantaneous collector current and collector-emitter voltage during the transistor's transition from the ON and OFF state. As stated before, power losses during the turning ON of the transistor are neglected due to the natural commutation of current from the anti-parallel diode to its corresponding transistor. Therefore, only losses associated with turning OFF the transistor will be considered.

The transistor losses are modeled by the transistor turn-OFF characteristics shown in Figure 4.1. Assuming the collector current i_C exhibits a linear fall with a the fall time t_F, the approximation for the turn-OFF losses $P_{Q,TURN-OFF}$ for both transistors is expressed as

$$P_{Q,TURN-OFF} = 2V_Q \, i_X (T_S/2) \, t_F \qquad (4.11).$$

Using equation (2.15) or (2.16), the value for the instantaneous current at the time of transistor turn OFF is easily calculated. All other variables in equation (4.11) are predetermined, thus computation of $P_{Q,TURN-OFF}$ is quite simple. Combining the results for the switching and conduction losses provides total component losses for the switching transistors P_Q, such that

$$P_Q = P_{Q,ON} + P_{Q,TURN-OFF} \qquad (4.12).$$

4.2 ANTI-PARALLEL DIODE LOSSES

Analysis for the losses in the anti-parallel diodes, D_1 and D_2 is similar to the analysis of power losses in the switching transistors; however, because of the relatively rapid turning ON and OFF of the diodes, it is assumed that the switching losses are negligible. Therefore, the only losses for the anti-parallel diodes requiring an expression are the conduction losses ($P_{D,ON}$).

As in the case of the switching transistors, it is assumed that when the diodes are ON, the voltage across the junction of the diode (V_D) is constant. Due to the half-wave symmetry of the L-C tank current i_x, the ON time current waveforms of the two diodes are identical. Therefore, the conduction losses for each of the diodes D_1 and D_2 are equal. The conduction losses in both diodes can be expressed as

$$P_{D,ON} = (2/T_s)V_D\int_0^{T_A} i_x(t)dt \qquad (4.13).$$

These limits of integration correspond with the diode conduction interval when the diode current is given by (2.15). Integration of (4.13) is equivalent to calculating the average anti-parallel diode current I_D. However, using

an analysis similar to the one used for calculating ON-time losses for the switching transistors will produce a simplified result.

From the expression for M in equation (4.4), subtracting the integer one from both sides of (4.4) results in,

$$M - 1 = -2I_D/(I_o + I_D) \qquad (4.14).$$

Substituting equation (4.7) into (4.14) and solving for I_D results in

$$I_D = nI_o(1 - M)/2 \qquad (4.15).$$

Substituting the expression for M (2.5) into (4.15), the final results for I_D are

$$I_D = I_o(n - V_o/V_g)/2 \qquad (4.16).$$

Therefore, the expression for conduction losses for both diodes, $P_{D,ON}$ is

$$P_{D,ON} = V_D I_o(n - V_o/V_g)/2 \qquad (4.17),$$

which is in terms of known design and user-defined

parameters. Since the conduction losses are the only losses considered for anti-parallel diodes, the total power loss for the anti-parallel diodes P_D is

$$P_D = V_D I_O (n - V_O/V_S)/2 \qquad (4.18).$$

4.3 RECTIFYING BRIDGE DIODE LOSSES

The expression for the loss in the four bridge diodes, DB_1-DB_4, P_{DB} is simplified by assuming losses due to turning ON and turning OFF are negligible due to the unforced commutation between each pair of diodes in the bridge. Another assumption is the ON voltage for each bridge diode V_{DB} is constant. By declaring all bridge diodes to be identical and knowing that the average current through each bridge diode is identical, the power losses in the bridge $P_{DB.ON}$ can be expressed as

$$P_{DB.ON} = 2V_{DB} I_O \qquad (4.19).$$

Since $P_{DB.ON}$ is the only loss considered for the bridge diodes DB_1-DB_4, the expression for P_{DB} is

$$P_{DB} = 2V_{DB} I_O \qquad (4.20).$$

An interesting observation is the expression for the

rectifying bridge loss P_{DB} is solely dependent on the diode voltage drop (V_{DB}) and the user-defined average output current I_O and is independent of the design variables R_O and n.

4.4 SERIES INDUCTOR LOSSES

Analysis of losses in the inductor P_L is divided into two sections. The first section is concerned with developing the expression for the inductor winding loss $P_{L,W}$. The second section is concerned with developing an expression for the inductor core loss $P_{L,C}$ which includes hysteresis loss, residual loss, and eddy current loss. Combining the two expressions results in a single expression for the total power losses in the inductor,

$$P_L = P_{L,W} + P_{L,C} \qquad (4.21).$$

The inductor winding resistive loss is expressed as a function of the winding resistance R_W and the root mean square (rms) value of the series L-C circuit current I_{XRMS}, such that

$$P_{L,W} = I_{XRMS}^2 R_W \qquad (4.22).$$

The winding resistance can be expressed as a function of the number of turns on the inductor N_L, the mean length per turn l_w, the copper resistivity p, the window area of the core A_w, and the fill factor k_w, such that

$$R_w = N_L^2 l_w p/(k_w A_w) \qquad (4.23).$$

Solution of equation (3.4) provides the value of the inductor L for a particular set of user-defined variables and design variables n and R_D. For a specific magnetic core with permeability μ, cross sectional area A_c, and mean path length of the magnetic core l_c, the number of turns on the inductor N_L can be computed as

$$N_L = [L l_c/(A_c \mu)]^{1/2} \qquad (4.24).$$

Now that the expression for the winding resistance has been determined, an expression for I_{xrms} is required.

The definition of the rms value of a periodic function f(t) is

$$rms = [(1/(T)) \int f^2(t)\, dt]^{1/2} \qquad (4.25).$$

To determine the rms value for i_x, the following integration is required,

$$I_{xRMS} = [(2/T_S) \int i^2_x(t)\, dt]^{1/2} \qquad (4.26).$$

Using the expression for i_x in equations (2.15) and (2.16) and the expression for T_A (2.12), equation (4.26) is converted to

$$I_{xRMS} = (V_S/R_O)((2/T_S)[\int_0^{T_A}((1 + MK + M)\sin(w_O(t - T_A)))^2\, dt + \int_{T_A}^{T_S/2}((1 + MK - M)\sin(w_O(t - T_A)))^2\, dt])^{1/2} \qquad (4.27).$$

Performing the operations prescribed in equation (4.27) results in

$$I_{xRMS} = (V_S/R_O)((1/T_S)[(1 + MK + M)^2(T_A + (1/2w_O)\sin(2w_O(- T_A))) + (1 + MK - M)^2(T_S/2 - T_A - 1/(2w_O)\sin(2w_O(T_S/2 - T_A)))])^{1/2} \qquad (4.28).$$

Combining the results of equations (4.23) and (4.28) and substituting into (4.22) provide an expression for the inductor winding losses $P_{L.w}$.

The second type of loss in the inductor L considered is the inductor core loss $P_{L.c}$. Victor E. Legg expressed the total inductor core loss $P_{L.c}$ at low flux densities as an

equivalent AC core resistance $R_{L,C}$ [7]. Legg's equation (4.29) expresses the equivalent resistance $R_{L,C}$ as the sum of three inductor core loss factors: the hysteresis loss factor $R_{L,H}$; the residual loss factor $R_{L,R}$; and the eddy current loss factor $R_{L,E}$; such that

$$R_{L,C} = R_{L,H} + R_{L,R} + R_{L,E} \qquad (4.29).$$

The hysteresis loss factor is the product of the core permeability μ, the series inductor value L, the switching frequency f_s, the maximum flux level B_M, and an experimentally-obtained hysteresis loss coefficient a, such that

$$R_{L,H} = aB_M\mu Lf_s \qquad (4.30).$$

The residual loss factor $R_{L,R}$ is the product of the magnetic core permeability μ, the series inductor value L, switching frequency f_s and an experimentally-obtained hysteresis residual loss coefficient c, such that

$$R_{L,R} = c\mu Lf_s \qquad (4.31).$$

The eddy current loss factor $R_{L,E}$ is the product of the magnetic core permeability μ, the series inductor value L, the square of the switching frequency f_s, and an

experimentally-obtained eddy current loss coefficient e, such that

$$R_{L.E} = e\mu L f_s^{\,e} \qquad (4.32).$$

As stated earlier, the summation of equations (4.30) through (4.32) provide the value of the equivalent core resistance $R_{L.C}$, which multiplied with the square of the rms value series L-C circuit current results in the expression for inductor core loss, where

$$P_{L.C} = R_{L.C} I_{xRMS}^{\,e} \qquad (4.33).$$

The only variable in the expression for $P_{L.C}$ that has not been previously determined is the maximum flux level B_M. From electromagnetic theory, the expression for the maximum flux level B_M is a function of the core permeability μ, the number of turns on the inductor N_L (4.24), the mean path length of the magnetic core l_C, and the peak of the L-C tank current I_{xP} (2.18) or (2.20), where

$$B_M = \mu N_L I_{xP} / l_C \qquad (4.34).$$

An expression for the both inductor core and winding

losses, and ultimately an expression for the total inductor loss in terms of known design and circuit parameters has been developed.

4.5 SERIES CAPACITOR LOSSES

The model used to represent the non-idealities of the series capacitor C is shown in Figure (4.2). The model consists of an effective series inductance (ESL), the capacitance C, an effective parallel resistance (EPR) which models the dissipative quality of the charged capacitor, and the effective series resistance (ESR). In the analysis of capacitor power losses, the effects of the ESL and EPR are neglected. The only parasitic element to be considered is the ESR. Therefore the expression for total capacitor losses P_C is

$$P_C = I_{xRMS}^2 ESR \qquad (4.35),$$

where the value of I_{xRMS} is expressed in equation (4.28) and the value of ESR is determined experimentally.

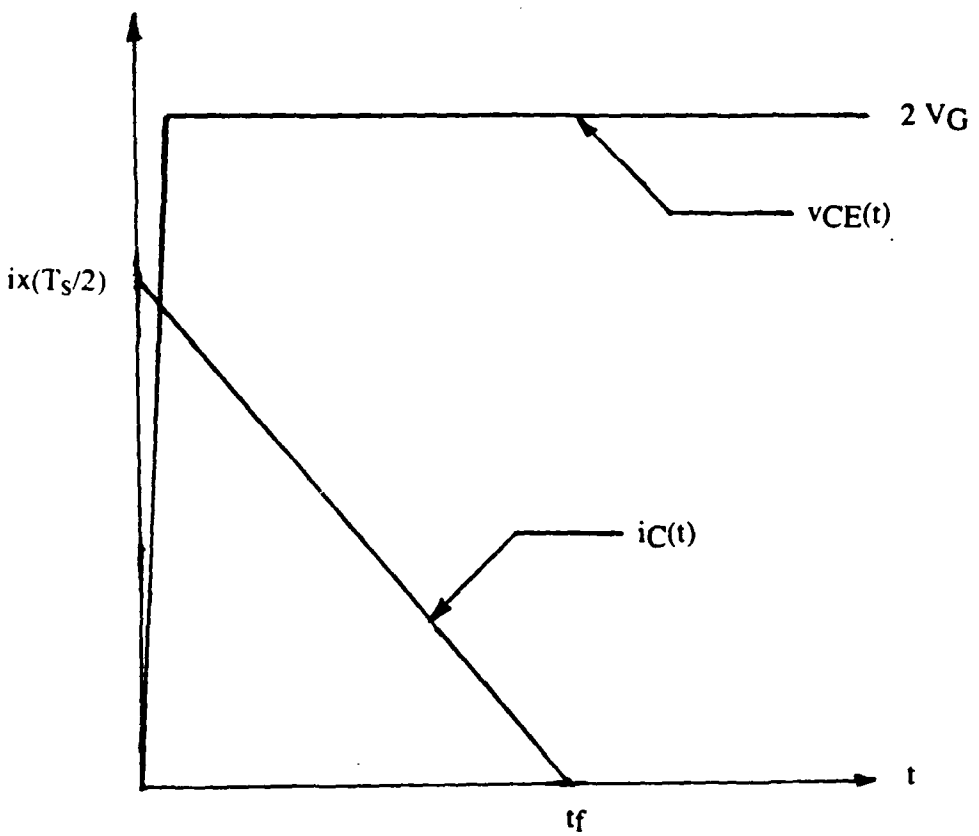


Figure 4.1 Transistor Switching Loss Model

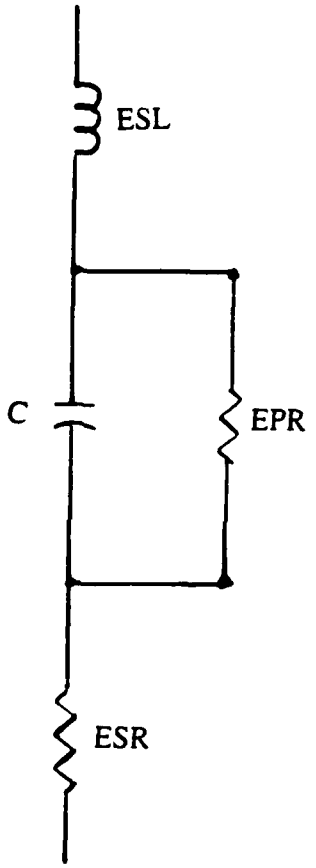


Figure 4.2 Non-Ideal Capacitor Model

CHAPTER 5

RESULTS AND EVALUATION OF DESIGN METHODS

In the previous chapter, analytical expressions were developed for the determination of individual component losses. The total component loss P_{TOTAL} is the summation of the individual component losses and is expressed as

$$P_{TOTAL} = P_Q + P_D + P_{DB} + P_L + P_C \qquad (5.1).$$

The expression for operating efficiency η of the series resonant converter (SRC) is

$$\eta = (1 - P_{TOTAL}/V_O I_O) \times 100\% \qquad (5.2).$$

In this a chapter, the operating efficiency of a hypothetical SRC circuit is presented as a function of the transformer turn ratio n and the characteristic impedance R_O. A brief explanation of results and a presentation of design strategies follows.

5.1 ANALYTICAL RESULTS

In order to use the expressions developed in this thesis to evaluate SRC operating efficiency, certain circuit parameters and user-specified dependent variables

must be given. The dependent circuit parameters for the hypothetical SRC circuit are given in Table 5.1.

Using the variables given in Table 5.1, the computer program presented in Appendix A is used to calculate the efficiency utilizing the expressions developed in Chapter 4. Figure 5.1 depicts the three-dimensional plot of the efficiency as function of the ordered pair (n,R_o) for values of n between 0.5001 and 0.7758 and values of R_o between 0.0500 and 6.262.

Figure 5.1 shows that for a particular value of n, there exists a maximum value of efficiency and a corresponding value for the changing characteristic impedance R_o. Evaluation of the individual component losses will help explain the occurrence of the maximum value of efficiency for the individual value of n. The easiest method of analyzing the three dimensional efficiency plot is to traverse the plot on a constant transformer turn ratio n line analyzing the individual component losses as a function of the characteristic impedance R_o.

There are several elements of the component losses that are independent of R_o and stay constant for a particular value of n. The first is the loss in the bridge diodes P_{D_B}

which is expressed in equation (4.20) as a function of the output current I_o and the forward voltage drop of the diode V_{DD}. For this hypothetical SRC circuit, P_{DD} is 14W, which represents 14% of the 100W output power of the total converter. Other types of losses that are independent of R_o are the conduction losses in the switching transistor $P_{Q,ON}$ (4.10) and anti-parallel diode $P_{D,ON}$ (4.17). The summation of the conduction losses in these two components effect the efficiency of the hypothetical SRC are totally dependent on the transformer turn ratio n, but not R_o.

Although the losses due to $P_{Q,TURN-OFF}$ (4.11) and $P_{L,C}$ (4.33) are dependent on R_o, their effects on efficiency are quite negligible. With an output power of 100W, theses losses, $P_{Q,TURN-OFF}$ and $P_{L,C}$ are typically 1.5W. However, at extremely high values of R_o and n, these losses become significant. The factor causing the greatest fluctuation in the efficiency is the losses due to the parasitic resistances which include the inductor winding resistance R_w and the effective series resistance (ESR) of the capacitor. At turn ratio n, as the increasing values of characteristic impedance R_o relate to increasing values of inductance L. This increasing inductance produces lower values of I_{xRMS}. The increase in inductor value limits the variation of the L-C tank current i_x about its zero average value, consequently reducing the value of I_{xRMS}. However,

the reduction in rms current does not necessarily result in a decrease in resistive losses. The value of R_w is increased due to the increase in the number of turns N_L required to produce the value of inductance L specified. The effects of the decreasing I_{xRMS} and increasing resistance R_w on the resistive losses P_{REST} at a particular value of n as a function of R_o are shown in Figure 5.2. Figure 5.2 shows a distinct operating point where resistive losses are minimized. The shape of the curve in Figure 5.2 shows the direct effects of the value of R_o on the occurrence of a maximum efficiency point for a particular value of n.

5.2 DESIGN STRATEGIES AND RECOMMENDATIONS

When designing an SRC for above-resonance excitation, several general rules apply. Operating the SRC with a normalized voltage conversion ratio M close to unity reduces the conduction losses of the switching transistor and anti-parallel diodes when the ON voltage of the diode is significantly greater than the transistor's ON voltage. The input voltage range of the dual voltage sources V_{s1} and V_{s2} in Figure 2.1 determines the value of the transformer turn ratio n required to provide the constant output voltage V_o and output current I_o. When maximizing

converter efficiency, the value of n is determined from the operating conditions; the value of R_o is chosen to minimize the losses for that particular value of n. When certain circuit parameters are unknown or cannot be experimentally determined, the value of R_o should be selected to minimize the resistive power losses since the resistive losses have the strongest effect on optimum efficiency point.

A number of enhancements can be made to future versions of this analysis which may improve the estimation of total power losses of the SRC. A recommendation is to include circuit parasitics in the expressions used in the oesign method. Inclusion of the voltage drops of the switching devices and bridge diodes in the derivations of the expressions for the current waveforms can perhaps provide more accurate values of normalized voltage conversion ratio M. Defining the output voltage V_o as

$$V_o = I_o R_L \qquad (5.3),$$

the adjusted normalized voltage conversion ratio M' which includes ON-time voltage drops, is expressed as

$$M' = (V_o + 2V_{DB})/n[V_o - qV_D - (1 - q)V_{o.ON}] \qquad (5.4),$$

where q is a weighting factor between 0 and 1/2. Substituting the values of M' from (5.5) for the normalized voltage conversion ratio M in equation (3.1) will result in new values of f_o, L, and C for a given set of user-defined dependent variables and ordered pair (n,R_o).

Other recommendations include:

a) the development of additional expressions for the transformer core and winding power losses,

b) the adjustment of the value of circuit inductance L to compensate for the effective series inductance (ESL) of the capacitor,

c) the analysis of the effect of inductor core material and dimensions on SRC efficiency, and

d) the development of an expression for inductor core losses operating at high magnetic flux densities due to the fact that Legg's equation (4.29) is valid in magnetic core applications involving low magnetic flux densities.

5.3 CONCLUSION

A method for analyzing SRC operating efficiency has

been presented. Included in the analysis is the development of expressions relating operating efficiency to the design variables n and R_o, and given circuit parameters. The operating efficiency is graphically represented as a function of the n and R_o for a hypothetical SRC circuit followed by a brief explanation of the results and possible enhancements to the proposed design method.

Table 5.1 User-Defined Dependent Variables

Circuit Dependent Variables

V_S = 20V V_O = 10V I_O = 10A f_S = 50kHz

Transistor Specifications

V_{CESAT} = 0.2V $t_f = 50 \times 10^{-9}$ sec

Diode Specifications

$V_D = V_{DD} = 0.7V$

Inductor Core Specifications

μ_R = 26 vol = 22.69×10^{-6} m^3 $A_C = 0.1990 \times 10^{-3}$ m^2

l_C = .1074 m l_W = 0.0622 m $A_W = 0.426 \times 10^{-3}$ m^2

k_W = 0.2 a = 4.0×10^{-6} c = 96×10^{-6} e = 7.0×10^{-9}

Capacitor Specifications

ESR = 0.1 ohms

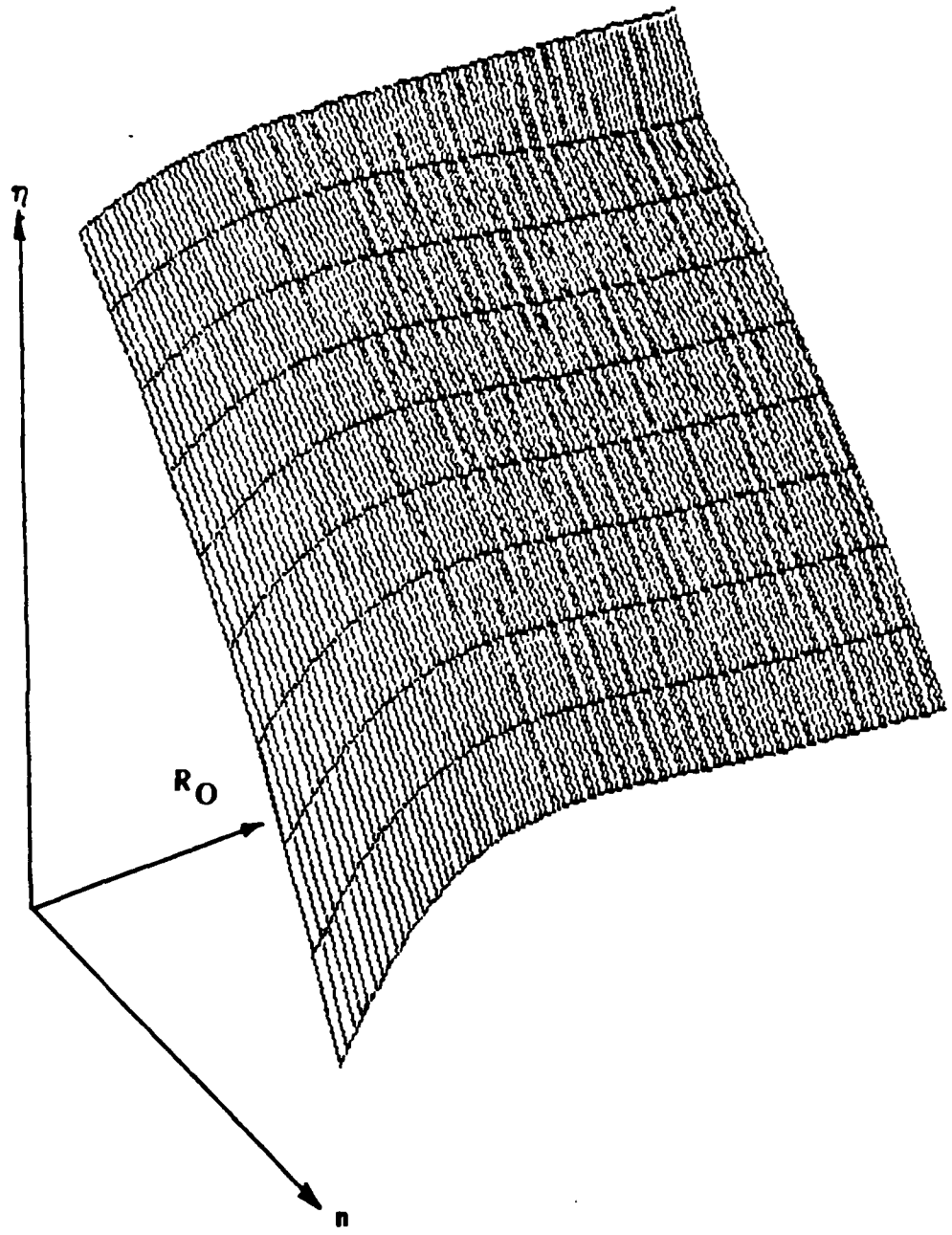


Figure 5.1 Three Dimensional Plot of SRC Efficiency

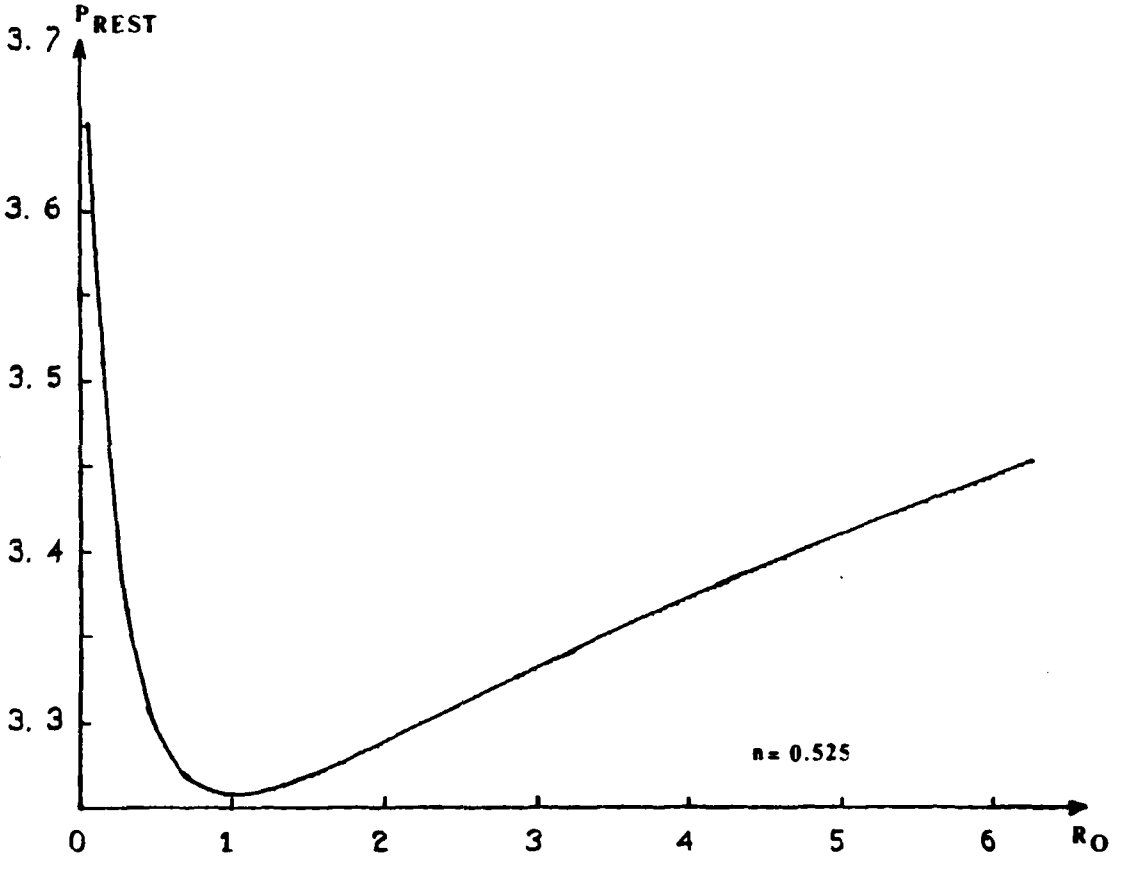


Figure 5.2 Resistive Losses-Versus-R_o

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[7] Victor E. Legg, "Magnetic Measurements at Low Flux Densities Using the Alternating Current Bridge," Bell System Technical Journal, Volume 15, January 1936, pp. 39-62.

Appendix A: Fortran Program Code

```
C     FRANCIS A. FAHY
C     FORTRAN PROGRAM COMPUTING LOSSES
C     FOR SERIES RESONANT CONVERTER
      PROGRAM LOSSES
      INTEGER II,III,IV,IIV,A,IIIV,AA
      REAL*4 PI,VG,FO,ROMEGA,L,C,TS,GAMMA,K,I,J,RO,LEN,AREA,
     *M,F1,VQ,VD,PDB,PQ,PD,PCOND,K1,K2,IRMS,IOFF,PTURNOFF,
     *N1,N,FS,TF,Z,ILP,PERM,VCP,VOL,TA,BMAX,PERMMAX,UR,B,
     *RHO,PTOTAL,PCORE,PREST,CSR,LPT,RAC,EFFIC,SRMS,AWIN,KWIN
      OPEN(UNIT = 6, FILE = 'B:MISCP.OUT', STATUS = 'NEW')
      OPEN(UNIT = 7, FILE = 'B:EFF.OUT', STATUS = 'NEW')
      OPEN(UNIT = 8, FILE = 'B:ILP.OUT', STATUS = 'NEW')
      OPEN(UNIT = 9, FILE = 'B:IRMS.OUT', STATUS = 'NEW')
C
C     The following constants are design parameters required
C     for the calculation of losses in the series resonant converter.
C     All parameter values labeled in MKS.
C
C     V is the ouput voltage, VG is the input voltage, VQ is the transistor
C     on-state voltage drop, VD is the diode on-state voltage drop, FS is the
C     switching frequency, I is the ouput voltage, UR is the relative
C     permeability of the core, VOL is the volume of the core,
C     BMAX is the maximum allowable fluctuation of the flux density,
C     LEN is path length of the core, AREA is the cross sectional area of the
C     core, RHO is the  resistivity of the transformer windings for Cu,
C     CSR is the capacitor series resistances,  LPT is the core winding
C     turn length, KWIN is the fill factor, and AWIN is the core window area.
C
C     GAMMA, the normalized switching frequency, is intialized at 1 x 10-5.
C
      WRITE(7,101)
  101 FORMAT('  N          RO          EFFICIENCY')
      WRITE(8,102)
  102 FORMAT('  N          RO          ILP         PCORE')
      WRITE(9,103)
  103 FORMAT('  N          RO          N1          IRMS        PREST')
      WRITE(6,104)
  104 FORMAT('  N          RO          PCOND       PTURNOFF')
        V = 10.00
        TF = 50E-9
        VG = 20.00
        VQ = 0.2
        VD = 0.7
        FS = 50E3
        I = 10.00
        UR = 26
        VOL = 22.69E-06
        BMAX = 0.20
        LEN = 0.1074
        AREA = 0.1990E-03
        RHO = 1.75E-08
        CSR = 0.1
        LPT = 0.0622
        AWIN = 4.26E-04
        KWIN = 2.0E-01
```

```
        PI = 3.14159
        N = 5.001E-01
        RO = 5E-02
C
C
      DO 100 A = 1,10
      DO 150 AA = 1,100
      M = V/(N * VG)
      J = RO * (N * I)/VG
C
C
C     SOLVE FOR GAMMA AS A FUNCTION OF M AND J
C
      GAMMA = .00001
      IF (M .EQ. 1.0) GO TO 5
      DO 30 II = 1, 3
        GAMMA =  GAMMA + 1E0
        CALL F(M,GAMMA,J,F1)
        IF (F1 .EQ. 0) GO TO 4
        IF (F1 .GT. 0) GO TO 1
 30   CONTINUE
      GAMMA = 3.2
 1    DO 40 III = 1,10
        GAMMA = GAMMA -  1E-1
        CALL F(M,GAMMA,J,F1)
        IF (F1 .EQ. 0) GO TO 4
        IF (F1 .LT. 0) GO TO 2
 40   CONTINUE
 2    DO 50 IV = 1,10
        GAMMA = GAMMA + 1E-2
        CALL F(M,GAMMA,J,F1)
       IF (F1 .EQ. 0) GO TO 4
       IF (F1 .GT. 0) GO TO 3
 50   CONTINUE
  3   DO 60  IIV = 1,10
        GAMMA = GAMMA - 1E-3
        CALL F(M,GAMMA,J,F1)
        IF (F1 .EQ. 0) GO TO 4
        IF (F1 .LT. 0) GO TO 6
 60   CONTINUE
 6    DO 70 IIIV = 1, 10
          GAMMA = GAMMA + 1E-4
          CALL F(M,GAMMA,J,F1)
          IF (F1 .GE. 0) GO TO 4
 70   CONTINUE
  5   GAMMA = PI
  4   FO = GAMMA * FS / PI
C
C
C     SOLVE FOR COMPONENT SIZE AND INDUCTOR TURNS N1
C
C
      PERM = UR * 1260E-09
      L = RO / (2E0 * PI * FO)
      C = 1/(2E0 * PI * FO * RO)
```

```
      K = J * GAMMA/(2E0 * M)
      N1 = SQRT(L * LEN / (AREA * PERM))
C
C
      TS = 1 / FS
      ROMEGA = 2E0 * PI * FO
C
C
C     COMPUTE TRANSISTOR TURNOFF LOSSES
C
      IOFF = ROMEGA * C * VG * SQRT((1 - M * M) * M * K * (M * K + 2E0))
      PTURNOFF = (2E0 * VG) * IOFF * TF / TS
C
C     COMPUTE PEAK CURRENT AND PEAK CAPACITOR VOLTAGE
C
      Z = 1 - M - (M * M) * K
      IF (Z .LE. 0E0) THEN
        ILP = ROMEGA * C * VG * (1 - M + M * K)
      ELSE
        ILP = IOFF
      END IF
C
      VCP = VG * M * K
C
C     COMPUTE MAXIMUM CORE PERMEABILITY
C
      PERMMAX = VOL * BMAX * BMAX/(L * ILP * ILP)
      IF (PERMMAX .LT. PERM) THEN
      EFFIC = 0
      GO TO 160
      ELSE
        GO TO 55
      END IF
C
C     COMPUTE FLUX DENSITY (B)
C
 55   B = PERM * N1 * ILP/LEN
C
C     COMPUTE CONDUCTION LOSSES IN SWITCHING DEVICES AND BRIDGE
C     IAVEOUT IS AVERAGE OUTPUT CURRENT
C
C
      PDB = 2E0 * VD * I
      PQ =  I * VQ * (1 + M) * N / 2E0
      PD = I * VD * (1 - M) * N / 2E0
      PCOND = PDB + PQ + PD
C
C     COMPUTE RMS CURRENT IRMS
C
      TA = (1/ROMEGA) * ACOS((1 + M *(1 + M * K))/(M *(K + 1) + 1))
C
      K1 = ROMEGA * C * VG * (1 + M * (K + 1))
      K2 = ROMEGA * C * VG * (1 + M * (K - 1))
      SIRMS = ( 2E0 / TS * (K1 * K1 *(0.5 * TA + SIN(-2E0 * ROMEGA *
     *TA)/(4E0 * ROMEGA)) + K2 * K2 *(0.5 * (TS / 2E0 - TA) - SIN(2E0 *
```

```
     *ROMEGA * (TS - TA)/(4E0 * ROMEGA ))
      IRMS = SQRT(SIRMS)
C
C     COMPUTE CORE LOSSES
C
      RAC = (7.0E-09 * FS * FS + 96E-06 * FS + 4.0E-06 * B * FS * 1E04)
     ** UR * L
      PCORE = RAC * IRMS * IRMS
C
C     COMPUTE RESISTIVE LOSSES (PREST)
C
      PREST = (N1 * N1 * LPT * RHO/(AWIN * KWIN) + CSE) * IRMS * IRMS
C
C     COMPUTE TOTAL POWER LOSSES
C
      PTOTAL = PCOND + PCORE + PREST + PTURNOFF
C
C     COMPUTE EFFICIENCY
C
      EFFIC = (1 - PTOTAL/(V * I)) * 100
      IF(EFFIC .LT. 0E0) THEN
      EFFIC = 0
      GO TO 160
      END IF
C
C     PRINT OUT VALUES
C
       WRITE(8,621) N,RO,ILP,PCORE
       WRITE(6,621) N,RO,PCOND,PTURNOFF
 621   FORMAT(4(E12.6,1X))
       WRITE(9,622) N,RO,N1,IRMS,PREST
 622   FORMAT(5(E12.6,1X))
 160   WRITE(7,620) N,RO,EFFIC
 620   FORMAT(3(E12.6,1X))
 151   RO = RO * 1.05
 150   CONTINUE
 111   N = N * 1.05
       RO = 5E-02
 100  CONTINUE
      CLOSE(UNIT = 6)
      CLOSE(UNIT = 7)
      CLOSE(UNIT = 8)
      CLOSE(UNIT = 9)
      STOP
      END
C
C     DEFINE SUBROUTINE TO SOLVE FOR GAMMA FROM
C     TRANSCENDENTAL EQUATION FOR M AND J
      SUBROUTINE F(XX,YY,ZZ,F1)
      DOUBLE PRECISION X,Y,Z,DIFF,AA,BB,CC
      REAL*4 F1,XX,YY,ZZ
      X = DBLE(XX)
      Y = DBLE(YY)
      Z = DBLE(ZZ)
      AA = Y/2D0
```

```
      BB = DTAN(AA) * DTAN(AA)
      CC = Z * AA
      DIFF = BB - ((X * X) * BB + (Z * Y) + (CC * CC))
      IF (DIFF .LT. 0D0) F1 = -1
      IF (DIFF .EQ. 0D0) F1 = 0
      IF (DIFF .GT. 0D0) F1 = 1
      RETURN
      END
```